

**In The Specification:**

Please substitute paragraph [0023] as follows:

[0023] To provide a deeper explanation of control chip operation, refer to the timing diagram in Fig. 3. In fact, Fig. 3 is a timing diagram showing various signal traces produced by the control chip according to the preferred embodiment of this invention. When SADDOUT transmits the actual address PA[31:25] in bit time zero, AIB01 of the bus interface unit 130 is refreshed. When SADDOUT transmits the actual address PA[24:12] in bit time one, AIB02 of the bus interface unit 130 is refreshed. Similarly, the content transmitted during bit time two will refresh AIB03 of the bus interface unit 130 and the actual address PA[34:32] and PA[11:3] transmitted during bit time three will refresh AIB04 of the bus interface unit 130. Note that frequency of AIBT01 of the bus interface unit 130 is half of SADDOUTCLK. Hence, after the bus interface unit 130 receives the actual address PA[31:12] at bit time zero and bit time one, the first section read address[31:12] of the memory read command is refreshed through Cqfc\_ReqAddr. As shown in label 310 of Cqfc\_ReqAddr in Fig. 3, the bus interface unit 130 coupled first section address read/compare unit 150 picks up the first section read address[31:12]. Thereafter, the first section read address[31:12] is compared with identical bit portion of write address of the memory-write commands inside the memory-write command queue to output a first comparison signal HHIT to the grant decision unit 170. If the first comparison signal HHIT indicates a mismatch between identical bits, the grant decision unit 170 submits a grant execution

signal MRQDREQ in bit time zero of the next command while a successive read command is followed, or the grant decision unit 170 submits a grant execution signal MRQDREQ immediately after the read command is totally received in bit time 3, as shown in label 320.

On receiving the grant execution signal MRQDREQ, the memory command control unit 180 transfers the memory read command into a memory read command queue 195. Alternatively, the signal DADS is enabled so that the actual address of the memory read command is placed on the KA bus and transmitted to a memory controller. In the meantime, the memory controller responds with a DNA signal.

Please substitute paragraph [0018] as follows:

[0018] FIG.3 is a timing diagram showing various signal traces produced by the control chip according to the preferred embodiment of this invention.

The paragraph numbers above are in accordance to the patent application publication No. US 2003/0167386 A1.